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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/542,830 | 07/20/2005 | Tatsumi Setomoto | 92478-4900 | 8650 |

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| EXAMINER | |
|---|---|
| CROWE, DAVID R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2112 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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| 3 MONTHS | 12/29/2006 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/542,830 | SETOMOTO ET AL. | |
| | Examiner | Art Unit | |
| | David R. Crowe | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____..

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/20/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear where the constant current circuit is formed, whether the circuit is formed on the substrate or the sub-substrate.

3. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the socket. Without the socket neither the specification nor the drawings provide for connecting the modules in parallel.

### *Double Patenting*

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140

F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1, 2 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,949,772 in view of Sakamoto et al (US 6,489,637). Claim 18 includes a substrate, light emitting diode bare chips, a feeder terminal [power supply terminal] and a drive circuit. The reference claim does not express the drive circuit as being a constant current luminous intensity circuit. Sakamoto however describes a constant current circuit "C" serving as a protection circuit [column 10, line 44]. Said protection circuit "C" can replace a driving circuit [column 6, line 11]. Therefore it would be an obvious variation as deemed by one of ordinary skill in the art to have a driving circuit be interchangeable with a luminous intensity circuit as defined as a constant current circuit, thus making claims 1 and 2 of the instant application obvious variants of the previously patented invention.

6. Claims 1,7 and 8 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1,2 and 11 of U.S. Patent No. 6,949,772 as applied to claims 1 and 2 of the instant application in view of Sakamoto.

Claim 1 is rejected under the grounds stated above.

Claims 7 and 8: In view of the combination of claim 1, the claims add a socket to be used as a heat sink. The reference in claim 11 states, "The card type illumination source is supplied with power from the connector and has the back surface of the substrate thereof contact thermally the receiving portion." The connector is structurally equivalent to a socket as well as being used as a heat sink. Claim 8 of the instant application further adds limitation to the substrate to include an insulating layer on top of a metal layer. The reference patent in claim 2 calls for "An insulating layer...being provided on the surface of the metal base substrate." It has therefore been shown the addition of a socket and layer limitations on the substrate do not distinguish the applied for claims from those previously patented.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1,2,13 are rejected under 35 U.S.C. 102(b) as being anticipated by Levy et al (US 5765940).

9. Claim 1: Levy anticipates an LED module with a substrate [5], an LED [7], a power supply terminal [11] and a current regulating assembly [9] functioning as a luminous intensity stabilization circuit in that the assemble [9] "provides for steady

current to the LEDs so as to assure constant non-flickering reliable operation" (column 5, line 56)

10. Claim 2: Levy anticipates current regulator [9] providing a constant current. (Column 55, line 44)

11. Claim 13: Levy anticipates using a zener diode in parallel with the 5 main strings of 9 LEDs. (Fig 3. column 4 lines 29-39)

12. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Yamamoto (US 2002/0088983).

13. Yamamoto anticipates a main substrate [4], a light emitting diode [2], a power supply terminal [6], and a control circuit [3] broadly interpreted to read on the luminous intensity stabilization circuit in that it controls the current to the LED which affects intensity and would inherently be stable for at least some period of time.

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

15. Claims 1 and 7 are rejected under 35 U.S.C. 102(e) as being unpatentable over Kim in view of Yamamoto.

16. Kim teaches (Fig. 1) a substrate [120] an LED bare chip [122] a power supply terminal [140 the transistor receives the voltage from he power supply] and a luminous intensity stabilization circuit (column 3, line 18). Kim further teaches a socket [110] connected to the power supply source via connector [130] and wire [102].

***Claim Rejections - 35 USC § 103***

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1, 2, and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Sakamoto et al (US 6489637).

19. Claims 1 and 2: Yamamoto teaches a main substrate [4], a bare chip light emitting diode [2] a power supply terminal [6] and a control circuit as interpreted to be a luminous intensity stabilization circuit. Yamamoto fails to teach explicitly a constant current circuit. Sakamoto teaches a constant current circuit as a driving circuit (Column 10, lines 44-48). It would have been obvious to use the circuit of Sakamoto to replace the circuit of Yamamoto because they both can provide a steady current to the LED to drive illumination.

Claims 4-5: As applied to the combination of claim 2 above, Yamamoto teaches a sub-substrate [5] made of resin (Para. [0029]) attached to the main substrate [4] which as best understood to contain the circuit [3].

Claim 6: Yamamoto discloses the claimed invention except for connecting the modules. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use multiple modules connected in parallel, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

20. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Sakamoto as modified in claim 2 in further view of Inoue et al (US 6975813).

21. As applied to the modified structure of claim 2, Yamamoto and Sakamoto fail to explicitly teach a constant voltage circuit. Inoue teaches a constant current circuit including a conventional constant voltage circuit (column 15, line 18). It would have been obvious to use a constant voltage circuit in combination with a constant current circuit to improve noise in attempting to achieve a steady illumination.

22. Claims 1-3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6924973) in view of Katogi et al. (US 2002/0114155).

23. Kim teaches (Fig. 1) a substrate [120], an LED bare chip [122] power supply terminal equivalent to a power supply line [102] and said substrate [120] with a PCB containing a constant voltage circuit and a constant current circuit. (Column 2 line 10) Kim fails to teach the LED configuration or the presence of current detection units or control units. Katogi teaches (Fig. 4) LED chips in series strings connected in parallel, with each having a current detection unit (PC1-3) and a control unit for adjusting the

current (CPU). It would have been obvious to add the extra circuitry to Kim in order to prevent unnecessary failure due to power surges affecting a sign such as lightening strikes.

24. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto as applied to claim 1 in view of Gaines (US 6998594).

25. Yamamoto fails to teach a thermal element. Gaines teaches a temperature-sensing device [column 3, line 27-41] where the current is reduced when the temperature rises above acceptable levels [column 4, line 30-39]. It would have been obvious to one of ordinary skill in the art to fit the module of Yamamoto with a thermal sensing device in order to maintain light characteristics provided by the chip, as it is known in the art for heat to negatively affect luminosity.

26. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claims 1 and 7 in view of Yamamoto in further view of Chang et al (US 2004/0264195)

27. Kim teaches all limitations of claims 1 and 7. Kim fails to teach a multi-layer substrate or a heat sink with the socket. Yamamoto teaches a multilayer substrate (Fig. 3) with insulating layers P [3] on top of metal layer [4]. Chang teaches (Fig. 1) an LED light source with a heat sink [14]. It would have been obvious to one of ordinary skill in the art to have a double layer substrate, as they are common in the art. It would also have been obvious to include a heat sink because it is known in the art that heat affects

the efficiency, life and luminosity of an LED. The claim provides no limitations to the socket for material or performance, and therefore it would only be necessary for the substrate to include a metal layer in contact with the socket, as heat will dissipate through all materials to one extent or another therefore providing a medium to emit heat.

28. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Sakamoto as modified in claim 2 in further view of Inoue et al (US 6975813) as applied to claim 3 in further view of Gaines.

29. As applied to a modified version of Yamamoto as described above in the rejection of claim 3, Yamamoto still fails to teach a thermal element or abnormality detection unit. Gaines teaches a temperature-sensing device [column 3, line 27-41] where the current is reduced when the temperature rises above acceptable levels [column 4, line 30-39]. It would have been obvious to one of ordinary skill in the art to fit the module of Yamamoto with a thermal sensing device in order to maintain light characteristics provided by the chip, as it is known in the art for heat to negatively affect luminosity.

***Conclusion***

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kobayashi et al (EP 1 059 678 A2)

Kobayashi et al (EP 1 059 668 A2)

Sakamoto et al (US 6489637)

| | |
|---|---|
| Deese | (US 2003/0112627) |
| Friend | (US 6659623) |
| Shimizu et al | (US 2005/0207165) |
| Okuno | (US 4298869) |
| McGrogan et al | (US 3784844) |
| Robel et al | (US 5939839) |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David R. Crowe whose telephone number is 571-272-9088. The examiner can normally be reached on 7:30AM-5:00PM w/first Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jayprakash N. Gandhi can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

David R Crowe
Examiner
Art Unit 2112

DRC

JAYPRAKASH GANDHI
SUPERVISORY PATENT EXAMINER